REMARKS

The Office action of October 2, 2002 has been carefully considered, and applicants thank the Examiner for the thoroughness of the Office action. In the Office action, the title was objected to, and claims 1-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Reneris, U.S. Patent No. 5,903,894 (hereinafter Reneris) in view of Sescila III et al., U.S. Patent No. 5,937,175 (hereinafter Sescila). Claims 24-27 were objected to as being dependent on a rejected base claim, but were indicated as being allowable if rewritten in independent form, including the limitations of the base claim and any intervening claims. By the present amendment, a new title has been presented, claims 1, 9-11, 13-15 and 25 have been amended, and new claims 28-48 have been added. Applicants submit that the amendments were for purposes of clarification, and not for reasons related to patentability. The rejections are traversed in view of the following remarks, and reconsideration is respectfully requested.

Applicant thanks the Examiner for indicating that claims 24-27 contain allowable subject matter. Applicants have added new independent claims 33 and 40 which each recite the limitations of claims 24 or 25, respectively, along with the limitations of the base claim and any intervening claims. Applicants submit that these claims and those dependent thereon are thus allowable.

Turning to the rejection on the art, the present invention is generally directed towards dynamically determining, from the description of a computer system's configuration, whether machine resources (e.g., devices) need cycle (e.g., address and/or type) translation, and if so, then dynamically configuring those resources for translating bus cycles as appropriate. Translation can convert memory cycles to a I/O cycles and vice-versa, and/or memory cycles to other memory cycles with different addresses. In one implementation, ACPI technology is leveraged to obtain a

description of a computer system, including its bus data, bridge data, and so forth. This information is then analyzed to determine whether address translation for resources is needed, and when needed, the drivers of those resources provided with a translator (e.g., a table of functions) to properly perform the translation. Significant benefits result, including that the hardware abstraction layer (HAL) need not be changed for each different configuration of a machine. In other words, because the translation functionality is moved out of the HAL, which is very complex software and thus not desirable to customize, machines may be designed without being limited by how the HAL performs address translation, and/or without having to change the HAL. Note that the above description is for example and informational purposes only, and should not be used to interpret the claims, which are discussed below.

In contrast to the claims of the present invention, Reneris is generally directed towards providing an overall machine description, by converting a computer's description in one format, e.g., the byte stream data in differentiated definition blocks (DDBs) of ACPI, into a hierarchical data structure that is generally far more in a convenient and useable (than DDBs) when needed for referencing the machine's description. Significantly, there is nothing at all in Reneris teaching or suggesting that this hierarchical information might be used for dynamic resource translation, let alone for the recited concept of "determining from the description whether cycles output by a resource require translation from one bus to another bus." Because Reneris does not consider the concept of determining cycle translation in even a very a general way, there is clearly no sufficient teaching or suggestion in Reneris as to how the claimed invention might be accomplished, or even why it might be desirable to do so.

Thus, although the present invention may analyze such a general hierarchical structure to arrive at the resource translation requirements and translation information, the present invention as

claimed does significantly more than provide the machine description as disclosed in Reneris. In fact, the claims essentially recite that the computer system's description is used to make a determination as to translation, and also to dynamically configure the resources (e.g., their drivers) for cycle translation when determined to be needed. In other words, Reneris is only describing one tool that may be used by the present invention, but does not disclose each of the claim limitations that the Office action contends that Reneris discloses.

For example, the Office action alleges that the text of column 12, lines 34-55 of Reneris is directed to "determining the description of the device and providing the translation for the resource and configuring the resource based on the translator." Office action, page 2. However, this is a wholly incorrect interpretation of Reneris. First, a fair reading of Reneris shows that the only "translation" to which Reneris is referring is translating a byte stream of data within differentiated definition blocks (the DDBs) of ACPI into the hierarchical objects of the data structure. No reasonable interpretation of "translation" can be made by simply ignoring the surrounding context as to what is being translated, as the Office action appears to have done in interpreting claims 1 and 15. In fact, the very premise on which the Office action has based its rejection of claims 1 and 15, e.g., that the machine description of Reneris "provide[s] a translation for the resource and configure[s] the resource," is simply not supported by Reneris.

Further, *providing* a hierarchical description of the device, which is essentially what Reneris is describing at column 12, lines 34-55, is not the same as *determining* something from such a description, and certainly not anything that reasonably teaches or suggests "determining from the description whether cycles output by a resource require translation from one bus to another bus, and if so, providing a translator for the resource," as recited in claim 1, for example. It appears that the Office action has clearly misinterpreted what Reneris has actually described, namely

translating "the byte stream of data within the DDB" to create a hierarchy, which is wholly unrelated to translated cycles as claimed.

At the same time, Sescila is directed to coupling remote instrumentation via a serial bus to a PCI device, with translation between that serial bus and the PCI bus. Such a configuration will always need translation, and thus, like Reneris and in direct contrast to the claims, there is nothing in Sescila related to determining whether a translation is needed. Further, Sescila does not (and cannot) do this by a machine description, as the remote instrumentation described in Sescila is not part of the machine, but connected via the serial connection. Thus, although Sescila needs to perform some translation, like Reneris, Sescila simply does not teach or suggest configuring the resources dynamically for cycle translation based on any machine description.

By law, in order to establish prima facie obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In addition, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Thus, even if somehow permissible to combine Reneris with Sescila, (which applicants submit it is not, as discussed below), the claims of the present invention are not reached. Simply put, neither reference comes close to teaching or suggesting the concept of "determining from the description whether cycles output by a resource require translation from one bus to another bus, and if so, providing a translator for the resource and dynamically configuring the resource for translating cycles based on the translator" as recited in claim 1, or "a first component configured to analyze a description of the machine, and based on the description, to determine from the description whether cycles output by the resource require translation from one bus to another bus, and if so,

to dynamically provide a translator for the resource based on translation that will be performed at the bus bridge" as recited in claim 15. For at least the foregoing reasons, the claims are patentable over the prior art of record, whether considered alone or in any permissible combination as a matter of law. Reconsideration and withdrawal of the §103(a) rejections is respectfully requested.

Applicants also submit that the dependent claims are separately patentable over the prior art of record for numerous other significant reasons, however, because Reneris and Sescila are so seriously deficient in their teachings with respect to the independent claims of the present invention, only a few examples highlighting the apparently misunderstandings in the Office action's rejections will be discussed. For example, in rejecting claim 5, the Office action has cited a passage in Reneris directed towards interpreting the byte stream to build the machine description, which is wholly unrelated to evaluating a current resources object of the computer system's description, as defined in the specification and claimed. In rejecting claim 6, the only part of the machine description referred to in column 11, lines 11-30 of Reneris is related to power management features, which is clearly not "address translation information" as defined in the specification and claimed. Similarly, with respect to claim 7, there simply is no translator for a resource described in Reneris, let alone any teaching or suggestion of providing a translator that includes returning a table of functions, as essentially claimed. The rejection of claims 8 and 23 further emphasize the Office action's fundamental misunderstanding of the present invention and the prior art, in that column 15, lines 31-41 of Reneris are again referring to interpreting the byte stream to build the hierarchical machine description, and not to the translator for the resource. Applicants request reconsideration and withdrawal of the rejections of the dependent claims.

Further, as a matter of law, obviousness may not be established using hindsight obtained in view of the teachings or suggestions of the applicants. *W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). To guard against the use of such impermissible hindsight, obviousness needs to be determined by ascertaining whether the applicable prior art contains any suggestion or motivation for making the modifications in the design of the prior art article in order to produce the claimed design. The mere possibility that a prior art teaching could be modified such that its use would lead to the particular limitations recited in a claim does not make the recited limitation obvious, unless the prior art suggests the desirability of such a modification. *See In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

In the present case, the prior art is silent as to such a modification / combination, or anything remotely resembling how the present invention could be accomplished, or what might be accomplished thereby. Indeed, this is evident from the Office action's alleged motivation to combine, ("to leverage the large installation base of PCI devices and without modification"). Such a broad, unsupported statement has nothing to do with a machine description, let alone using it in the manner claimed, and applicants fail to see any relevance of this statement to any of the claims.

Instead of finding some proper motivation to combine, the Office action has only made one mere conclusory statement generally directed to PCI-based devices. Such a mere, conclusory statement does not come close to adequately addressing the issue of motivation to combine, are not evidence of obviousness, and therefore are improper as a matter of law. *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). It thus appears that the Office action selected Reneris simply for its references to the machine description, and Sescila simply for its reference to PCI-to-serial bus translation, in a (failed) attempt to reach the claims. It is clearly

evident that the Office can only have located Reneris and Sescila via impermissible hindsight gleaned from applicants' own teachings, and thereafter attempted to piece together the prior art's teachings into applicants' invention, even though when (impermissibly) combined, the recited subject matter is still not reached. For at least these additional significant reasons, applicants submit that the §103(a) rejections are improper as a matter of law, and respectfully request reconsideration and withdrawal of the rejections.

CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that claims 1-48 are patentable over the prior art of record, and that the application is good and proper form for allowance. A favorable action on the part of the Examiner is earnestly solicited.

If in the opinion of the Examiner a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney at (425) 836-3030.

Respectfully submitted,

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APPENDIX A
(marked up copy of the claims amended herein)

1. (Amended) A computer-implemented method [for performing resource translation], comprising:

obtaining a description of a machine;

determining from the description whether cycles output by a resource require translation from one bus to another bus, and if so, providing a translator for the resource; and

dynamically configuring the resource for translating cycles based on the translator.

9. (Amended) The method of claim 1 wherein providing a translator for the resource includes returning cycle type information.

10. (Amended) The method of claim 1 wherein the cycle type information corresponds to I/O.

11. (Amended) The method of claim 1 wherein the cycle type information corresponds to memory.

13. (Amended) The method of claim 1 wherein dynamically configuring the resource based on the translator includes telling a driver of the resource what cycles to issue to cause an appropriate I/O cycle on the other bus.

14. (Amended) The method of claim 13 further comprising starting a driver of the resource.

15. (Amended) A system for configuring a resource to communicate with a device, comprising:

a bus bridge to which the device is connected,

a first component configured to analyze a description of the machine, and based on the description, to determine from the description whether cycles output by the resource require translation from one bus to another bus, and if so, to dynamically provide a translator for the resource based on translation that will be performed at the bus bridge; and

a second component configured to obtain the translator from the first component, and further configured to tell the resource to output translated cycles based on information in [to] the translator.

25. (Amended) The system of claim 15 wherein the first component provides the translator to [changes] change a cycle type.

CERTIFICATE OF MAILING

I hereby certify that this Amendment and Petition for Extension of Time, along with Transmittal and Change of Correspondence Address in Application, are being deposited with the United States Postal Service on the date shown below with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Date: February 26, 2003

Albert S. Michalik

2420 amendment